UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,924	07/11/2003	Frederick George Fellenser	TN264	4226

7590 06/07/2006

Unisys Corporation
Attn: Michael B. Atlass
Unisys Way, MS/E8-114
Blue Bell, PA 19424-0001

EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,924	FELLENSER ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/18/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 14-25, 29-37, 39-54, and 57-58* is/are rejected.

7)☒ Claim(s) *11-13,26-28,38,55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 11-13, 26-28, 38, 55-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 14, 17-25, 29, 32-37, 41-42 and 45-54 rejected under 35 U.S.C. 102(b) as being anticipated by Baxter et al. (US 6,122,756).

In regard to claim 1, Baxter et al. disclosed an apparatus, comprising:

a multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* that uses cache coherency (*cache coherency, col. 9 lines 5-11)* for accessing memory (*memory subsystem, fig. 3, 252, col. 9 lines 5-11)*; and

a maintenance interface unit (*local resources, fig. 3, 260)* integrated (*each motherboard contains all the local resources that are required of the system, fig. 3, 202, col. 10 lines 27-39)* within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* configured to

(i) provide a backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* on-behalf of a peripheral maintenance system (*local resources, fig. 3, 260)* and

(ii) perform operations (*MC ASIC controls the execution of physical memory operations, fig. 3, 276, col. 9 lines 12-17)* within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* while participating in the cache coherency (*cache coherency, col. 9 lines 5-11).*

In regard to claim 2, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the apparatus includes one or more chips (*motherboard 0-7, fig. 2, 202, col. 8 lines 27-45).*

In regard to claim 3, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the backdoor interface (*RI, fig. 3, 306)* is integrated on a chip (*a chip on a motherboard, fig. 3, 306)* comprising part of the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)*, and the peripheral maintenance system (*I/O subsystem, fig. 3, 254)* is coupled to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* via the backdoor interface (*RI, fig. 3, 306)*, but is not integrated on the same chip (*I/O subsystem and local resources are integrated on a motherboard and connected through system bus,*

fig. 3) as the backdoor interface (*RI, fig. 3, 306).*

In regard to claim 4, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to read and/or write to memory while maintaining cache coherency (*MC ASIC managed both the directory and system coherency, fig. 3, 276, col. 9 lines 12-17).*

In regard to claim 5, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to communicate with one or more operating systems (*JP will send a message to the microcontroller on its board, col. 26 lines 62-66)* functioning in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 6, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured (*Board Master JP run "tertiary test" for all off-board JP and memory diagnostics, col. 25 lines 64-67 and col. 26 lines 1-6)* to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to initialize (*test suite I/O initialization testing, col. 25 lines 52-55)* the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 7, Baxter et al. disclosed the apparatus as recited in claim 1, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured to automatically notify the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* if an error condition is detected (*JP is not taken out of reset, col. 26 lines 57-61)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 8, Baxter et al. disclosed the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes recognizing when a device and/or operating system is not available (*motherboard is put back into reset, col. 26 lines 50-53)* and automatically notifying the multiprocessor system of the unavailability (*motherboard/daughter board that fail the diagnostic tests are deconfiguration and logged in NOVRAM configuration tables, col. 26 lines 18-21).*

In regard to claim 9, Baxter et al. disclosed the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes recognizing when a device and/or operating system is not available (*run diagnostic testes to ensure that motherboard meets the minimum requirements to function correctly, col. 26 lines 18-28)*, automatically notifying the multiprocessor system of the unavailability (*if motherboard has been determined bad at any point during the scan test, message is placed in the scannable mailbox to inform the master controller, col. 23 lines 46-58)*, and automatically notifying the peripheral

maintenance processor (*Job processor, JP, fig. 3, 250)* of the unavailability (*JP stay in reset mode, col. 26 lines 57-61).*

In regard to claim 10, Baxter et al. disclosed the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes issuing an interruption command to the multiprocessor system (*if the error is determined to be fatal, computer system is put in save system information mode, col. 7 lines 45-57).*

In regard to claim 14, Baxter et al. disclosed the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes performing error testing (*microcontroller is responsible for interconnect and ASIC testing, fig. 3, 300, col. 16 lines 59-61).*

In regard to claim 17, Baxter et al. disclosed a system, comprising:

a multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* that uses cache coherency (*cache coherency, col. 9 lines 5-11)* for accessing memory (*memory subsystem, fig. 3, 252, col. 9 lines 5-11)*;

a peripheral maintenance system (*I/O subsystem, fig. 3, 254)*, configured to monitor performance (*computer system is monitoring of errors that may representative of a faulted components, col. 7 lines 26-32)* of the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* and service the

multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* if aberrations are detected with the performance (; and

a maintenance interface unit (*local resources, fig. 3, 260)* integrated (*each motherboard contains all the local resources that are required of the system, fig. 3, 202, col. 10 lines 27-39)* within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)*, configured to provide backdoor accessibility (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* on-behalf of the peripheral maintenance system (*I/O subsystem, fig. 3, 254)*, and perform operations (*MC ASIC controls the execution of physical memory operations, fig. 3, 276, col. 9 lines 12-17)* within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* while participating in the cache coherency (*cache coherency, col. 9 lines 5-11)*.

In regard to claim 18, Baxter et al. disclosed the system as recited in claim 17, wherein the peripheral maintenance system (*I/O subsystem, fig. 3, 254)* is coupled to the multiprocessor system via the backdoor interface (*RI, fig. 3 306)* and is not integrated within the multiprocessor system (*I/O subsystem comprise of two independent PCI channels interfaced to the GG bus and communicate to job processor by bus packet, col. 9 lines s24-36)*.

In regard to claim 19, Baxter et al. disclosed the system as recited in claim 17, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to read and/or write to memory while maintaining cache coherency (*MC ASIC managed both the directory and system coherency, fig. 3, 276, col. 9 lines 12-17).*

In regard to claim 20, Baxter et al. disclosed the system as recited in claim 17, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to communicate with one or more operating systems (*JP will send a message to the microcontroller on its board, col. 26 lines 62-66)* functioning in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 21, Baxter et al. disclosed the system as recited in claim 17, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured (*Board Master JP run "tertiary test" for all off-board JP and memory diagnostics, col. 25 lines 64-67 and col. 26 lines 1-6)* to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to initialize (*test suite I/O initialization testing, col. 25 lines 52-55)* the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 22, Baxter et al. disclosed the system as recited in claim 17, wherein the maintenance interface unit (*local resources, fig. 3, 260)* is further configured

to automatically notify (*computer system is designed to include integrated JTAG test circuitry system/logic and scan chains that can be automatically performed by the system, col. 6 lines 40-43)* the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* if an error condition is detected (*JP is not taken out of reset, col. 26 lines 57-61)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 23, Baxter et al. disclosed the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes recognizing when a device and/or operating system is not available (*motherboard is put back into reset, col. 26 lines 50-53)* and automatically notifying the multiprocessor system of the unavailability (*motherboard/daughter board that fail the diagnostic tests are deconfiguration and logged in NOVRAM configuration tables, col. 26 lines 18-21).*

In regard to claim 24, Baxter et al. disclosed the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes recognizing when a device and/or operating system is not available (*run diagnostic testes to ensure that motherboard meets the minimum requirements to function correctly, col. 26 lines 18-28)*, automatically notifying the multiprocessor system of the unavailability (*if motherboard has been determined bad at any point during the scan test, message is placed in the scannable mailbox to inform the master controller, col. 23 lines 46-58)*, and automatically notifying the peripheral

maintenance processor (*Job processor, JP, fig. 3, 250)* of the unavailability (*JP stay in reset mode, col. 26 lines 57-61).*

In regard to claim 25, Baxter et al. disclosed the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes issuing an interruption command (*DIRQ_N,* to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 29, Baxter et al. disclosed the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit (*local resources, fig. 3, 260)* includes performing error testing (*microcontroller is responsible for interconnect and ASIC testing, fig. 3, 300, col. 16 lines 59-61).*

In regard to claim 32, Baxter et al. disclosed a multiprocessor system that uses cache coherency for accessing memory, a method comprising:

providing a backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* on-behalf of a peripheral maintenance system (*I/O subsystem, fig. 3, 254)*, the backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* integrated within the multiprocessor system (*highly available multi-*

processor computer system, fig. 2, 200, col. 8 lines 27-39) in the form of a maintenance interface unit (*local resources, fig. 3, 260)*; and

treating the maintenance interface unit (*local resources, fig. 3, 260)* as one of the processors (*microcontroller, fig. 3, 300)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* to enable participation in the cache coherency (*cache coherency, col. 9 lines 5-11)* .

In regard to claim 33, Baxter et al. disclosed the method as recited in claim 32, where treating the maintenance interface unit (*local resources, fig. 3, 260)* as one of the processor (*microcontroller, fig. 3, 300)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* further permits the maintenance interface unit (*local resources, fig. 3, 260)* to

(i) communicate with (*microcontroller assert a signal to the RI ASIC, fig. 3, 300, 306)*

(ii) issue commands to (*microcontroller test the bus through TEST BUS Controller, fig. 3, 300, 700)* and

(iii) monitor other devices and systems (*when the device detects a fault condition, it sets its DIRQ register bit and the interrupt is forwarded to the master microcontroller, col. 18 lines 35-43)* integrated (*computer system includes a group of three power supplies and three blowers, fig. 2, 210a-c, 212, col. 11 lines 23-40)* within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* while participating in the cache coherency (*cache coherency, col. 9 lines 5-11)* without having to interrupt the multiprocessor system (*highly available multi-processor computer*

system, fig. 2, 200, col. 8 lines 27-39).

In regard to claim 34, Baxter et al. disclosed the method as recited in claim 32, wherein providing the backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* and treating the maintenance interface unit (*local resources, fig. 3, 260)* as one of the processors (*microcontroller, fig. 3, 300)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* further permits the peripheral maintenance system (*I/O subsystem, fig. 3, 254)* to read, write, and initialize memory via the maintenance interface unit (*local resources, fig. 3, 260)* while participating in the cache coherency (*MC ASIC managed both the directory and system coherency, fig. 3, 276, col. 9 lines 12-17).*

In regard to claim 35, Baxter et al. disclosed the method as recited in claim 32, wherein providing the backdoor access comprises:

receiving an indication at the maintenance interface unit (*local resources, fig. 3, 260)* that a particular entity within the multiprocessor system is unavailable (*motherboard is deconfigured, col. 23 lines 31-45)*;

notifying the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* and the peripheral maintenance system (*I/O subsystem, fig. 3, 254)* of the unavailable entity (*JP and/or motherboard will be deconfigured when failed diagnostic test, col. 23 lines 30-45)*; and

responding (*no further communication with this address will be attempted, col. 21 lines 26-34)* to any messages sent to the unavailable entity (*motherboard with out*

acknowledge response, col. 21 lines 26-34) after receipt of the indication automatically.

In regard to claim 36, Baxter et al. disclosed the method as recited in claim 32, wherein providing the backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* comprises permitting the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to communicate with one or more operating systems (*microcontroller, fig. 3, 300)* functioning in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 37, Baxter et al. disclosed the method as recited in claim 32, wherein providing the backdoor access (*JP (daughter board) runs RI register access using backdoor method, fig. 3, 250a-b, col. 27 lines 31-32)* comprises automatically (*diagnostic testing and evaluation can be automatically performed by the system, col. 6 lines 40-43)* notifying the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* if an error condition is detected (*computer system is monitoring of errors that may representative of a faulted components, col. 7 lines 26-32)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 41, Baxter et al. disclosed one or more computer-readable media comprising computer executable instructions that, when executed, direct a peripheral computer to:

communicate (*I/O transfer, col. 9 lines 28-36)* with a cache coherent (*cache coherency, col. 9 lines 5-11)* multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* via a backdoor interface (*RI, fig. 3, 306)* embedded within the multiprocessor system (*embedded within one of the motherboard, fig. 3)*;

access memory in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* while simultaneously participating in cache coherency (*MC ASIC managed both the directory and system coherency, fig. 3, 276, col. 9 lines 12-17)* of the multiprocessor system (*MC ASIC managed both the directory and system coherency, fig. 3, 276, col. 9 lines 12-17)*; and

issue commands (*microcontroller issue command to JP whether to go onto the next stage, become a slave JP and go into idle loop, col. 27 lines 52-55)* to the backdoor interface (*RI, fig. 3, 306)* and receive information from the backdoor interface (*RI, fig. 3, 306)* relating to monitoring and maintaining performance (*computer system is monitoring of errors that may representative of a faulted components, col. 7 lines 26-32)* of the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 42, Baxter et al. disclosed one or more computer-readable media as recited in claim 41, further comprising computer executable instructions that, when executed, direct the computer to display information on a display device (*microcontroller prints a message to the system console, fig. 3, 300, col. 22 lines 43-45)* with respect to monitoring and maintaining the performance (*computer system is*

monitoring of errors that may representative of a faulted components, col. 7 lines 26-32) of the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 45, Baxter et al. disclosed one or more computer-readable media as recited in claim 41, further comprising computer executable instructions that, when executed, direct the computer to receive error conditions (*message is placed in the onboard scannable mailbox to inform the master microcontroller that an error was taken, col. 22 lines 65-67)* detected (*microcontroller put failed JP back to reset, col. 27 lines 43-47)* by the backdoor interface (*RI, fig. 3, 306)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 46, Baxter et al. disclosed an integrated within a cache-coherent multiprocessor system, a maintenance interface unit, comprising:

a transaction unit, configured to provide a backdoor access for a peripheral maintenance system (*I/O subsystem, fig. 3, 254)* to the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* and perform tasks on-behalf of a peripheral maintenance system (*I/O subsystem, fig. 3, 254)* in the multiprocessor system while participating in cache coherency of the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* without having to interrupt the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)*, wherein the peripheral maintenance

system (*I/O subsystem, fig. 3, 254)* is not integrated within the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)*; and

a housekeeping module configured to perform housekeeping operations in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)* automatically.

In regard to claim 47, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, further comprising an off-chip interface coupled to the peripheral maintenance system (*I/O subsystem, fig. 3, 254)*, configured to provide a communication link (*GG bus, fig. 3, 280)* between (*GG gatherer interrupts form motherboard and connected peripherals and directs them to the appropriate job processor JP by means of bus packet, col. 9 lines 32-36)* the peripheral maintenance system (*I/O subsystem, fig. 3, 254)* and the maintenance interface unit (*local resources, fig. 3, 260)*.

In regard to claim 48, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, further comprising an on-chip interface (*NCR SCSI, small computer interface, fig. 3, 284)* configured to provide a communication link (*PI Bus interface, fig. 3, 258)* between the maintenance interface unit (*local resources, fig. 3, 260)* and components integrated in (*components within the motherboard, fig. 3, 202)* the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39)*.

In regard to claim 49, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the transaction unit comprises a read/write module configured to permit (*microcontroller instructs JP and takes it out of reset to perform diagnostic tests, col. 27 lines 12-17)* the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to read and/or write to memory (*JP runs write/read tests, col. 27 lines 15-42)* while maintaining cache coherency (*cache coherency, col. 9 lines 5-11).*

In regard to claim 50, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an operating system module configured to permit (*JP waits for instruction from the microcontroller, col. 27 lines 12-14)* the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to communicate (*failed JP are reported to microcontroller for deconfiguration and put back into reset, col. 27 lines 43-46)* with one or more operating systems (*microcontroller, fig. 3, 300)* functioning in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 51, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an initialization module, configured (*Board Master JP run "tertiary test" for all off-board JP and memory diagnostics, col. 25 lines 64-67 and col. 26 lines 1-6)* to permit the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* to initialize (*test suite I/O initialization testing, col. 25 lines 52-55)* the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 52, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the housekeeping module (*local resources, fig. 3, 260)* comprises an error report module configured to automatically notify the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* if an error condition is detected (*JP is not taken out of reset, col. 26 lines 57-61)* in the multiprocessor system (*highly available multi-processor computer system, fig. 2, 200, col. 8 lines 27-39).*

In regard to claim 53, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the housekeeping module (*local resources, fig. 3, 260)* comprises a device notification module configured to recognize when a device and/or operating system is not available (*motherboard is put back into reset, col. 26 lines 50-53)* and automatically notify the multiprocessor system of the unavailability (*motherboard/daughter board that fail the diagnostic tests are deconfiguration and logged in NOVRAM configuration tables, col. 26 lines 18-21).*

In regard to claim 54, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the housekeeping module comprises a device notification module configured to recognize when a device and/or operating system is not available (*run diagnostic testes to ensure that motherboard meets the minimum requirements to function correctly, col. 26 lines 18-28)*, automatically notify the multiprocessor system of the unavailability (*if motherboard has been determined bad at any point during the scan test, message is placed in the scannable mailbox to inform the master controller, col. 23*

lines 46-58), and automatically notify the peripheral maintenance processor (*Job processor, JP, fig. 3, 250)* of the unavailability (*JP stay in reset mode, col. 26 lines 57-61).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 15-16, 30-31, 39-40, 43-44, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter et al. (US 6,122,756) in further view of Kitamorn et al. (US 6,728,668).

In regard to claim 15, Baxter et al. does not teach the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes injecting an error condition into the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

It would have been obvious to modify the system of Baxter et al. by adding Kitamorn et al. error injection for processor deconfiguration design verification. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would be advantageous for simulating errors in a processor within a multiprocessor system in order to test its system design and fault-tolerant recovery capabilities *(col. 1 lines 54-63).*

In regard to claim 16, Baxter et al. does not teach the apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes injecting a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Examiner interpret the artificial requests as equate to artificial error injected in to the multiprocessor system.

Refer to claim 15 for motivational statement.

In regard to claim 30, Baxter et al. does not teach the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes injecting an error condition into the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register (*fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 31, Baxter et al. does not teach the system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes injecting a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register (*fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 39, Baxter et al. does not teach the method as recited in claim 32, wherein the providing the backdoor access comprises injecting an error condition into the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 40, Baxter et al. does not teach the method as recited in claim 32, further comprising injecting a plurality of artificial requests into the multiprocessor system via the maintenance interface unit.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 43, Baxter et al. does not teach one or more computer-readable media as recited in claim 41, further comprising computer executable instructions that, when executed, direct the computer to issue a command to the backdoor interface to inject an error condition into the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 44, Baxter et al. does not teach one or more computer-readable media as recited in claim 41, further comprising computer executable instructions that, when executed, direct the computer to issue a command to the backdoor interface to inject a plurality of artificial requests into the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 57, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an error generation module, configured to issue artificial error messages within the multiprocessor system to enable the peripheral maintenance system to perform error testing.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

In regard to claim 58, Baxter et al. disclosed the maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an injection module, configured to inject a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.

Kitamorn et al. disclosed the method and apparatus for simulated error injection wherein the runtime error inject module simulates the processor hardware error by setting an appropriate error bit in error condition register *(fig. 5, 504, col. 7 lines 5-16).*

Refer to claim 15 for motivational statement.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER

Loan Truong
Patent Examiner
AU 2114